System Aware ESD Design

System Mindset For A Better Foundry

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Samsung Electronics, Foundry

Biography

- Career
  - Started EE Career at ON Semiconductor in March 2008 as design intern
  - ON Semiconductor ESD discrete device & process designer, 2009 - 2017
  - Samsung Electronics, HQ, Foundry Division, ESD verification, 2017 - present
- Education
  - B.S.E in electrical engineering in 2009, Arizona State University
  - M.S.E in electrical engineering in 2015, Arizona State University
- Pastime
  - Swing dancing, canyoneering, church, and my six children

Abstract

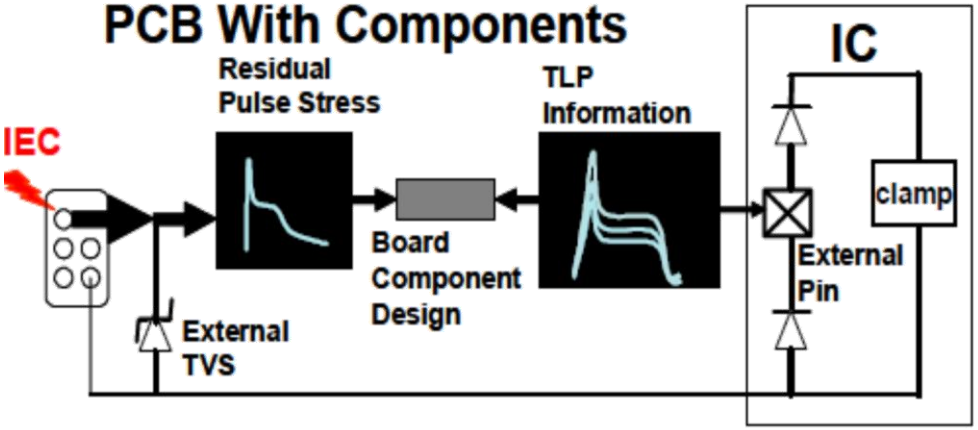
- With the increased complexity of ESD needs and the blurring of the lines between system and IC protection there has become a need for hybrid protection schemes relying on both on-chip and off-chip ESD devices to achieve ESD / EMC requirements. [1]
- Because of the interaction between system and IC ESD protection, an understanding of system needs over merely meeting specs is needed
- Existing trial and error and spin the silicon again approaches are costly and time consuming.
- It is proposed that by taking a system aware approach to ESD IC design and verification, potential ESD failures can be found resulting in less time and money while improving customer confidence.
- By identifying the actual pulse seen at the device pad, verification of designs using advanced analysis tools can more effectively be employed
- In order for foundries to become most trusted among their customers additional support and system level knowledge outside the normal expectations are needed.

Objectives

- Outline the ideal and real world of ESD design and verification
- Give an overview of how knowing the system can improve the ESD design and verification process at both the system and IC level
- Review a case study of how testing a customer supplied board can improve the ESD verification process

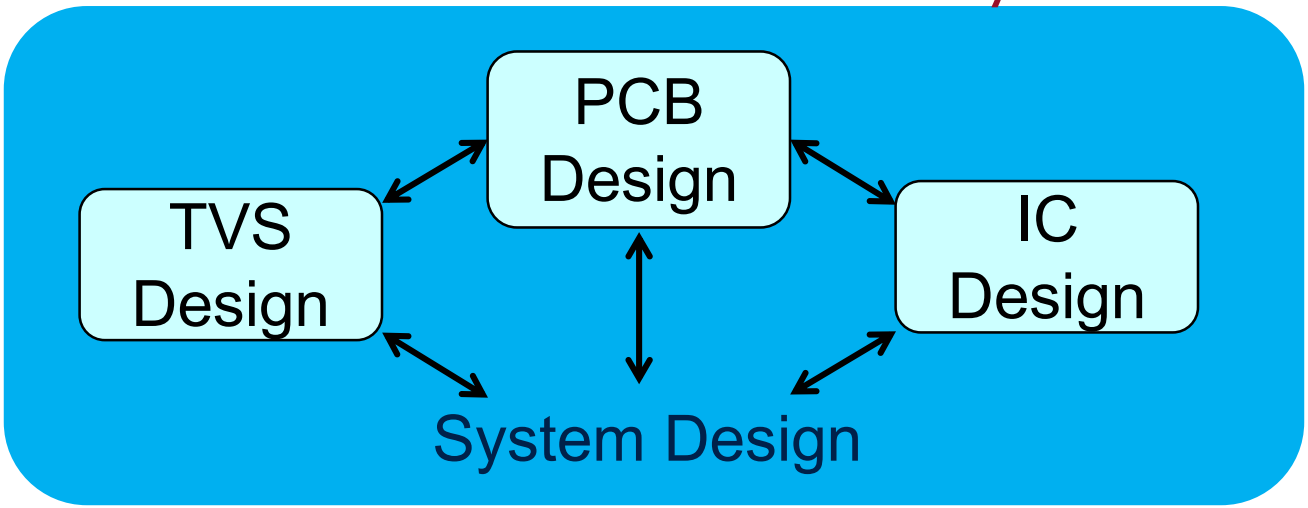
System Efficient ESD Design

- A foundry's place in the SEED approach



[2]

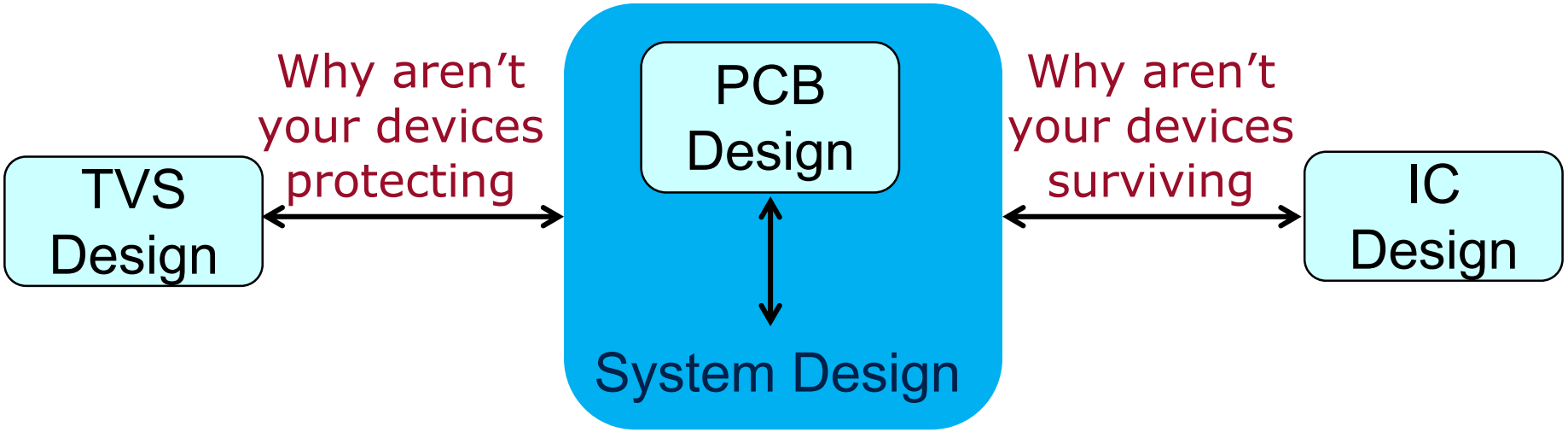
But where's the foundry?



The Reality Of ESD Design

- ESD protection is considered in system design
  - Not as co-design, but as specs to meet

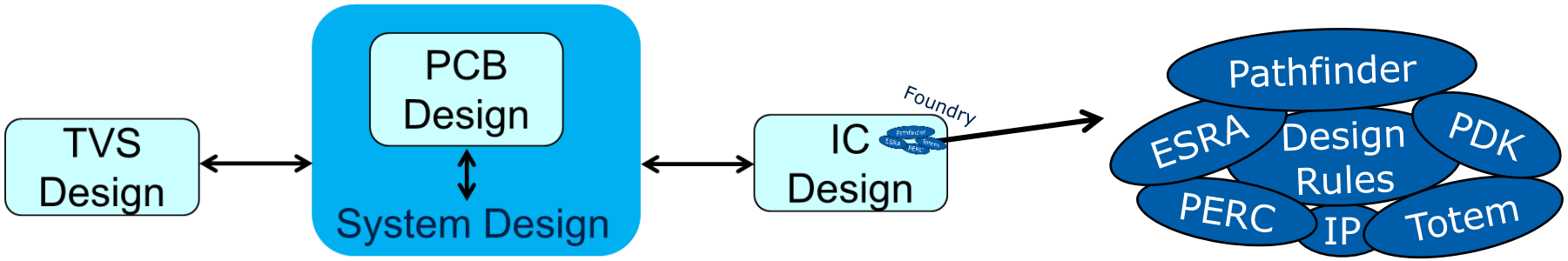
- Clear understanding and needs are still a mystery to customers



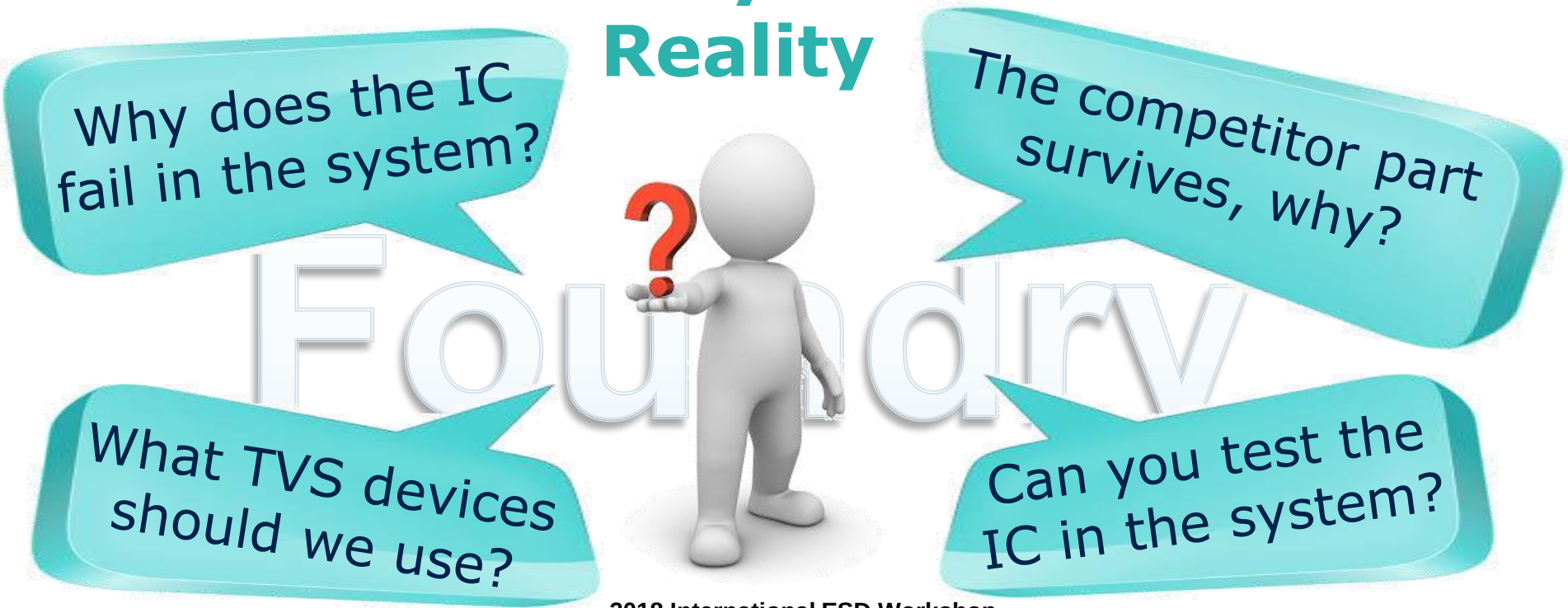
But still where's the foundry?

The Foundry Roll in ESD

- Perception: Generate PDK / run verification / make suggestions



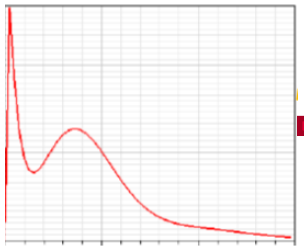
The System Reality



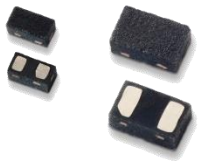
System Requirements ≠ IC Specs

- Customers often impose system and chip requirements without understanding of actual needs
- The wrong Reasons
  - The competitor survives more so meet it…
  - Greater the IC survival means greater the system survival…
- Not know what to design to can be the real problem

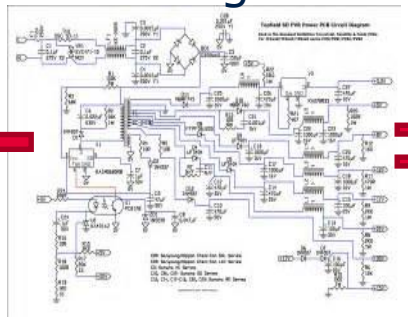
High system requirements



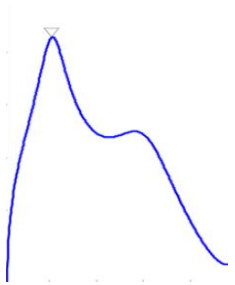
Inadequate System Protection



Non-Optimal Design



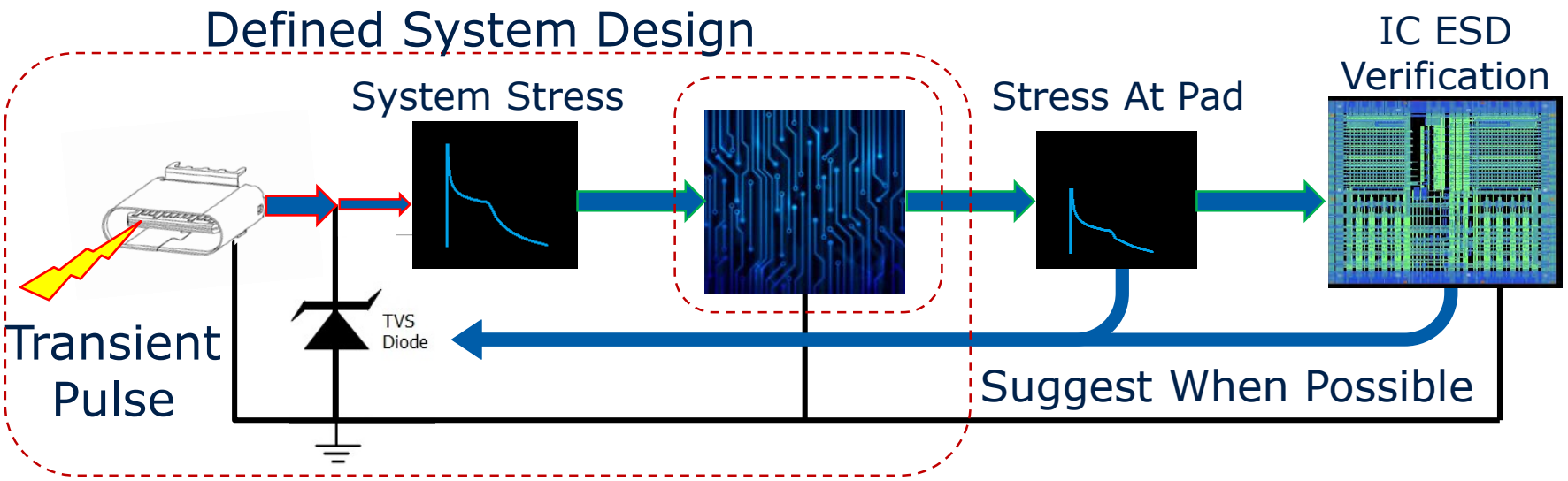
Higher Current At IC Pad



ESD Needs

System Aware ESD Verification / Design

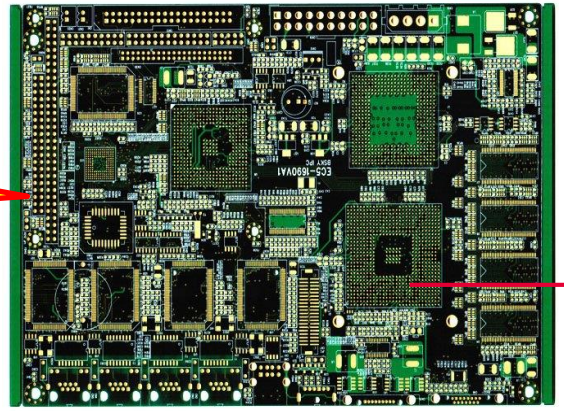
- When the system can't be changed…
  - Get more info than just specs
  - Know how much protection is needed
- Foundry verifies ESD performance on chip
  - Good inputs give info about IC survival and system needs



A Different Approach To Knowing What's Needed

- System Aware ESD Verification / Design Concept
  - Customers won't change, so we need to work smarter!
  - Not just designing IC specs, but system needs
- Better understanding of transient waveform distortion at IC pads – duration, peak current, etc.

System Requirement
TLP
or
IEC
External pins stressed

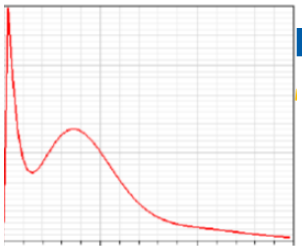


Current at pads measured

Vby1 Timing Controller Case

- Timing controller was developed and ESD verification completed
- When tested in the system there were pin failures
- Better understand upfront of system needs could have helped prevent need for failure analysis and resulting delays

System Requirements



System

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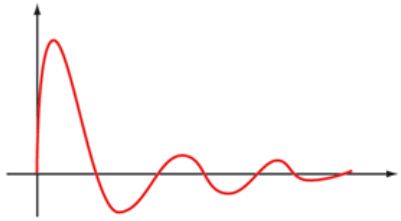
IC Specs



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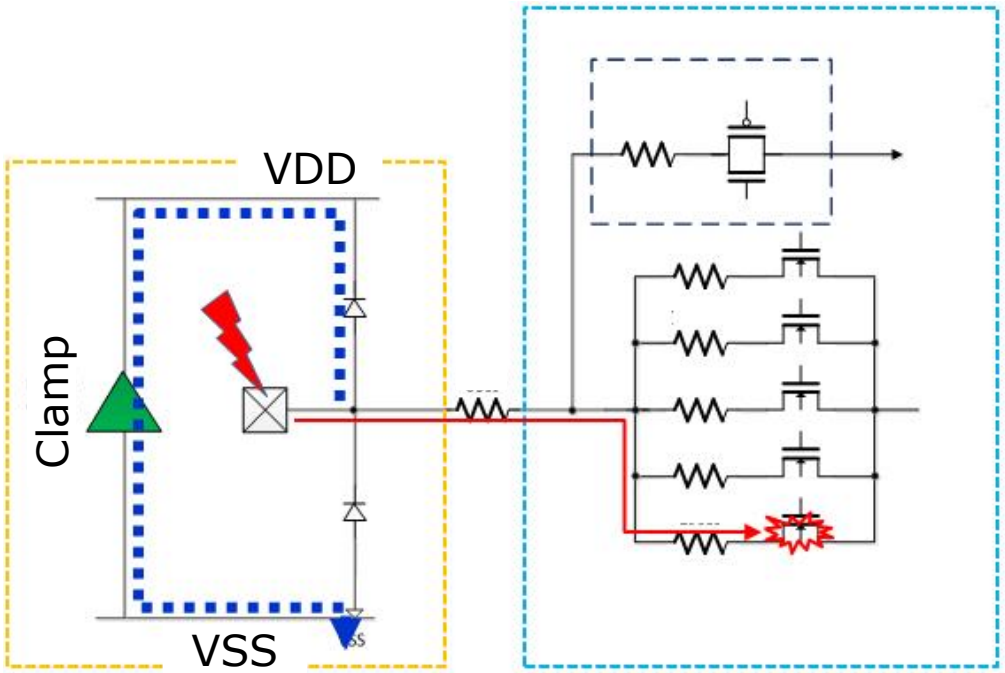
Pad Failures

Vby1 Timing Controller Case

- Typical ESD verification
  - Bump to Bump resistances, current density
- Calibrate measured peak current at pad to simulation to find potential weak points in device
  - Additionally, potential victim transistors

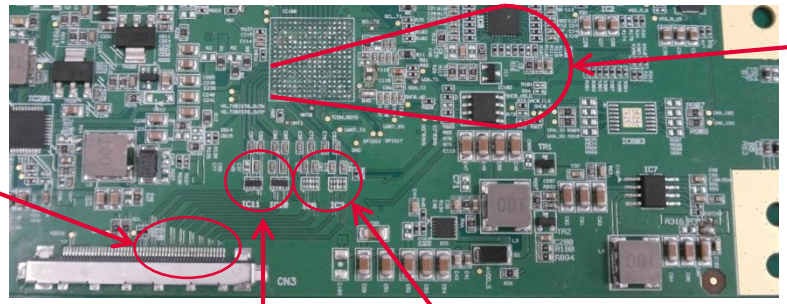
Bump to bump
Bump to clamp
Current density



Victim transistors
Vgs / Vds
violations

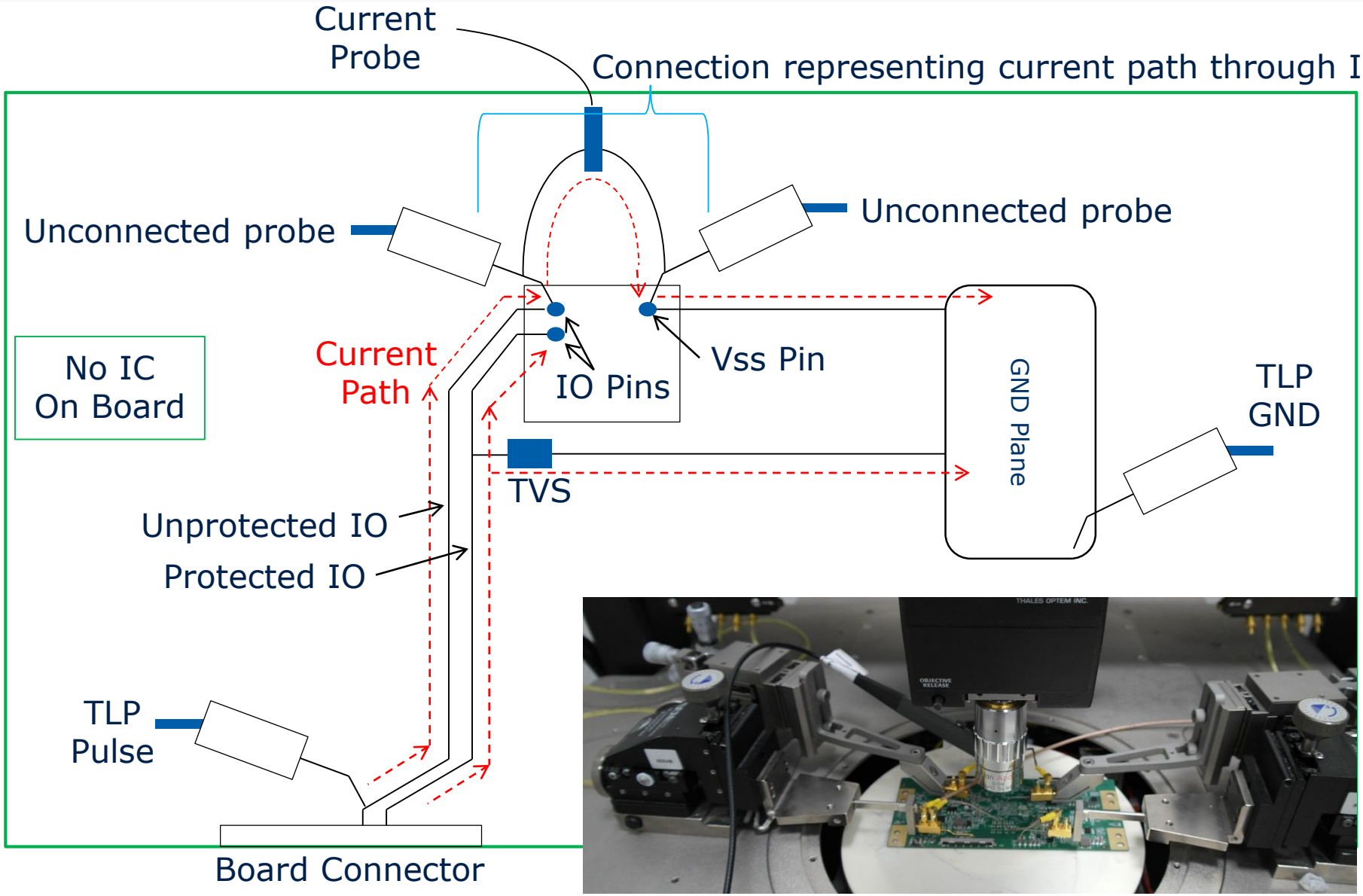
A Better Way

Vby1 Timing Controller Example Case

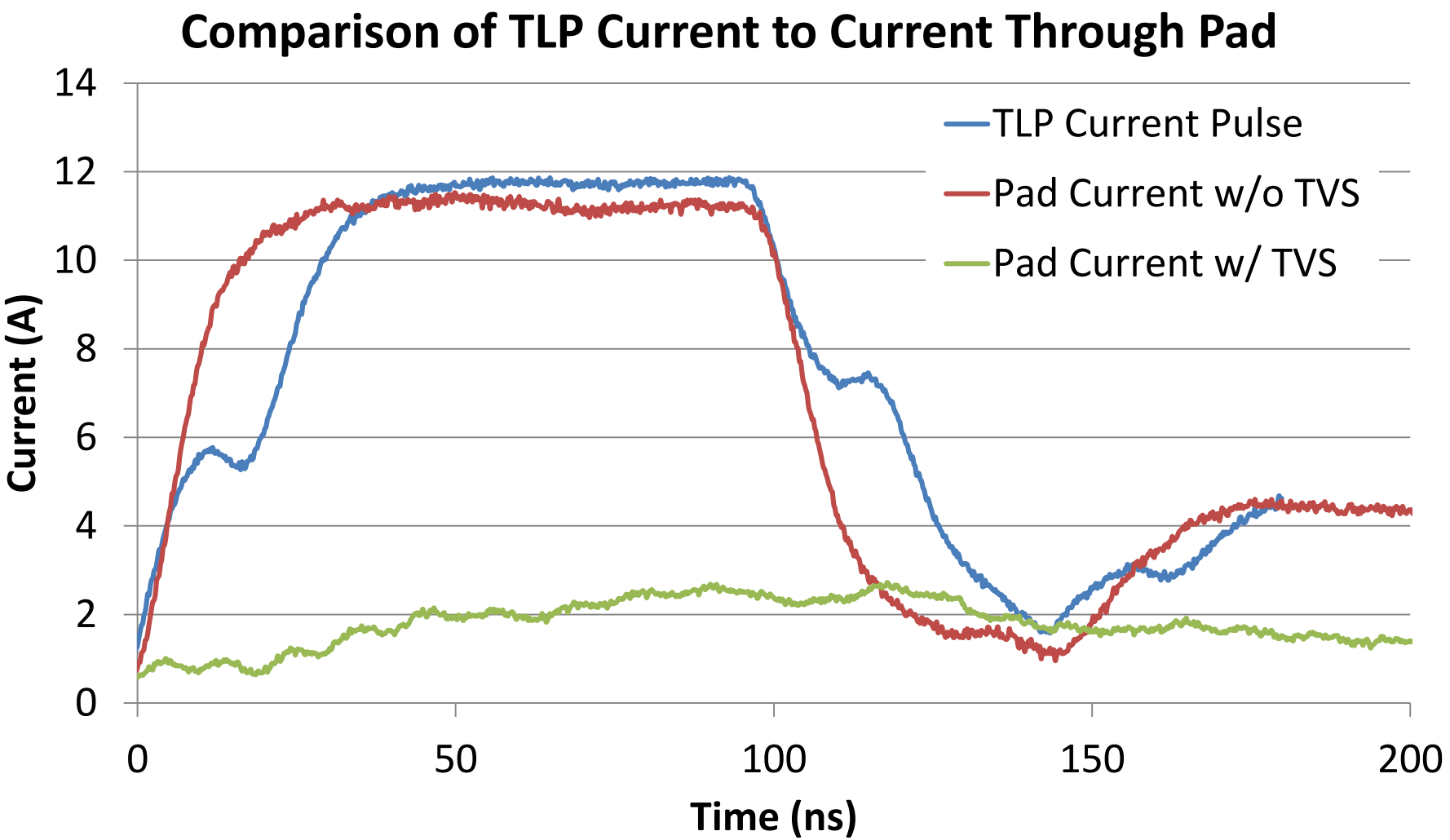


- System test methodology benefits
  - Gives system need for current at IC pads
    - Realistic input for ESD verification tools
  - Validate effectiveness of system ESD protection
  - Evaluate alternative system ESD solutions when possible

Measurement Test Setup

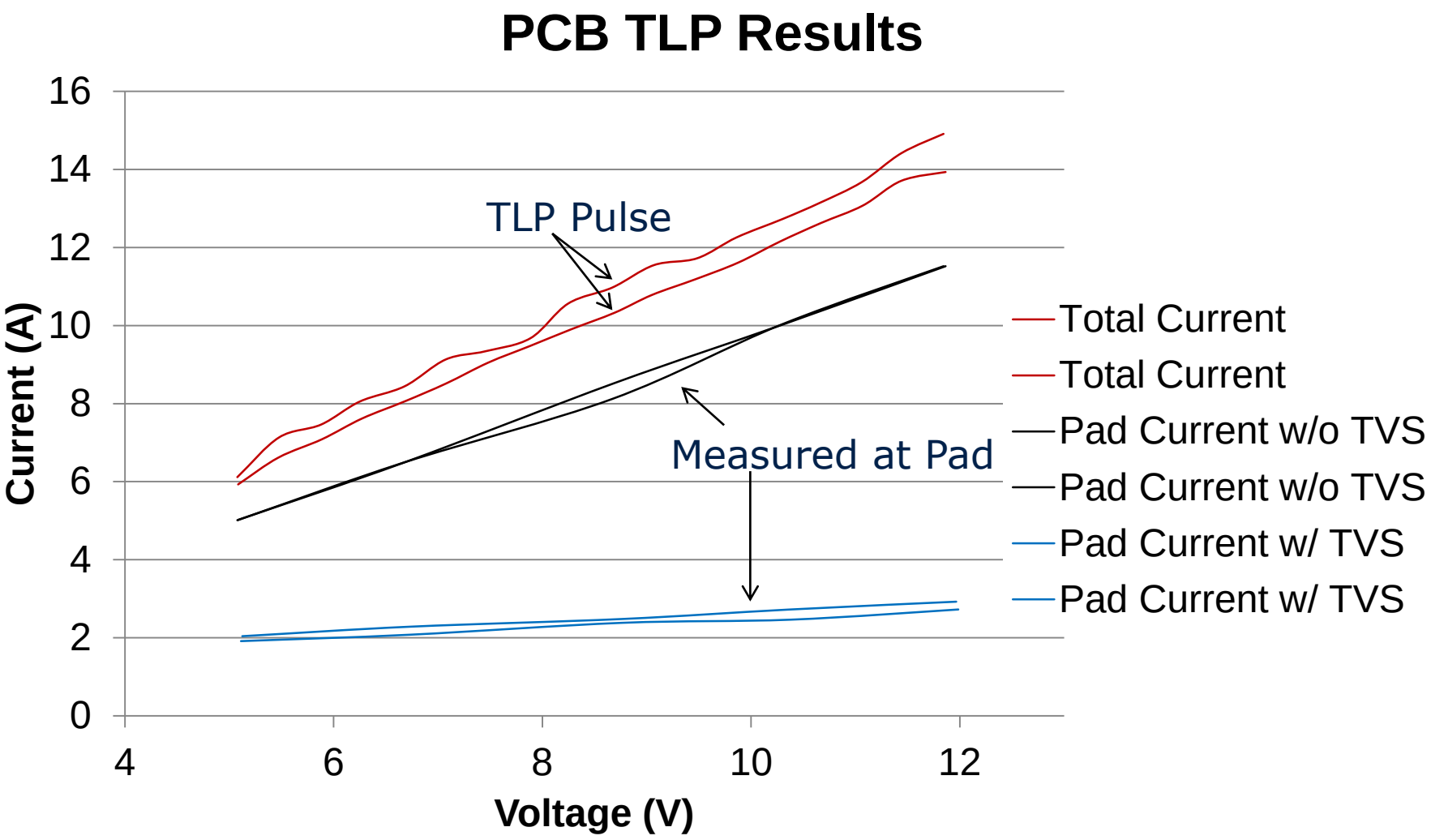


TLP Current Pulse



Measurements show actual current through the IC pad with ≈1/3 Ω resistance between IO and Vss

TVS Evaluation



TVS turns on and reduces current at the pad by 9A

Conclusion

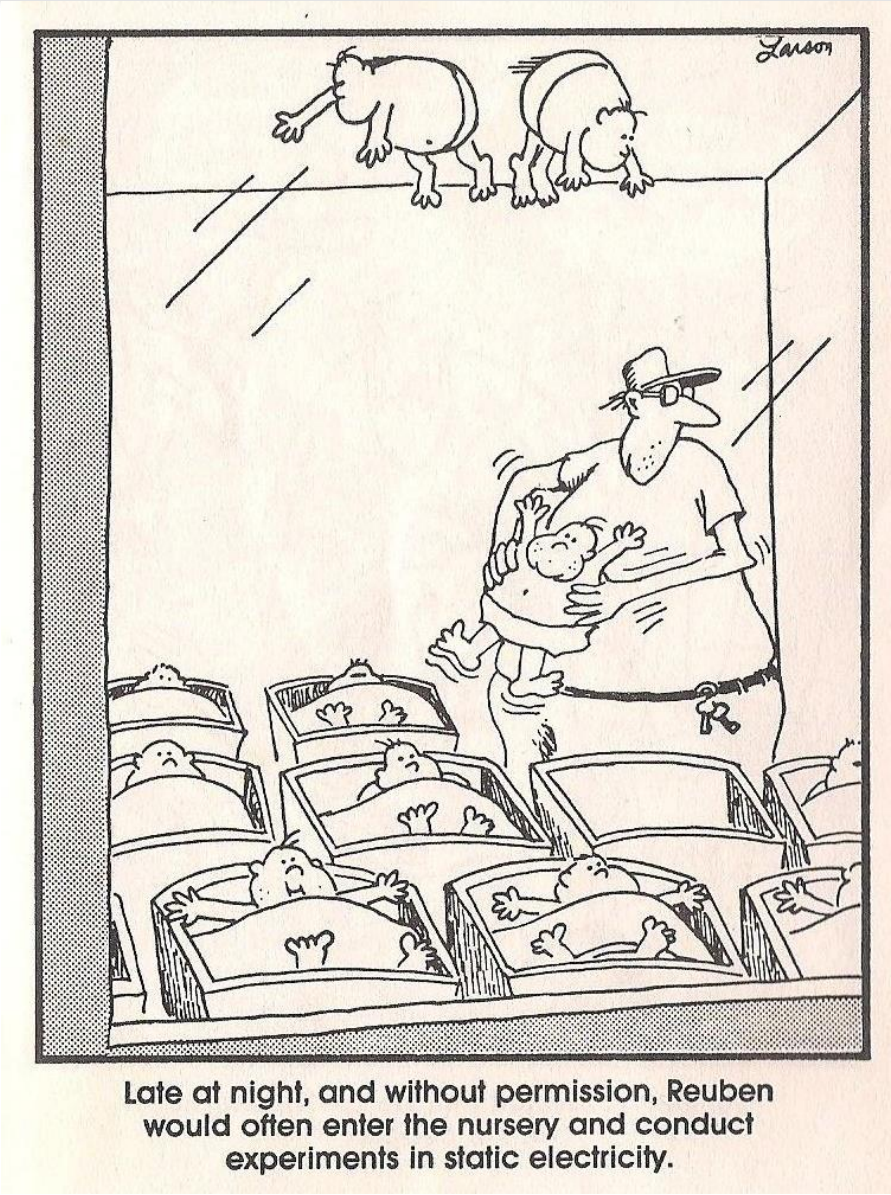
It was proposed that by measuring the waveform of a transient pulse applied to an electronic system, a system level spec such as IEC 61000-4-2 could be translated to usable input for IC ESD verification. 100ns TLP is well known for it's correlation factor of ≈ 2A / kV [3] thus making it well suited for supplying the injected transient to the system. The current waveform was then measured through the pad connections at the IC for a given IO to Vss path. This was measure with and without system level TVS ESD protection. In both cases, the peak current through IC pads had a linear relationship to the peak TLP current.

Conclusion

Given a know failure point of the IC pins, an estimate of the needed survival level of the IC could be determined for any system and system level protection. This information could also be used to validate the effectiveness of differing TVS devices.

By looking at the system that ICs are going into and gaining an understanding of what transient a device actually see, a foundry can provide more value to its customers in both guidance on system level protection as well as providing well designed and verified ESD solution at the IC level.

ESD Is No Laughing Matter…



[4]

References

1. G. Boselli, A. Salman, J. Brodsky and H. Kunz, "The relevance of long-duration TLP stress on system level ESD design," *Electrical Overstress/Electrostatic Discharge Symposium Proceedings 2010*, Reno, NV, 2010, pp. 1-10.
2. Industry Council White Paper 3 PI Rev1 Dec 2010
3. P. Besse, J. P. Laine, A. Salles and M. Baird, "Correlation between system level and TLP tests applied to stand-alone ESD protections and commercial products," *Electrical Overstress/Electrostatic Discharge Symposium Proceedings 2010*, Reno, NV, 2010, pp. 1-6.
4. Larson, Gary. "Farside." *The Complete Farside*. N.p.: Andrews, and McMeel, 2014. Print